What is claimed is:

1. A turbo code encoder for encoding at least one input set of *N* ordered permutation integers *I(k)*, where *k=1* to *N*, comprising:

a first encoder with memory size *m*, having a first input, coupled to a first source and a common source, and a multi-state register having 2^m states, for receiving said input bit set as said first source and encoding said input bit set to provide an encoded input bit set at a first output;

a hybrid S-random interleaver for receiving said input bit set and reordering the bits within said input bit set to provide a reordered input bit set, where S is an arbitrary predetermined value;

a second encoder with memory size *m*, having a second input, coupled to a second source and said common source, and a multi-state register having 2^m states, for receiving said reordered input bit set as said second source and encoding said reordered input bit set to provide a reordered encoded input bit set at a second output; and

a switch, for switching said first encoder from said first source to said common source and for switching said second encoder from said second source to said common source; whereby said first output provides said common source;

whereby said interleaver reorders said integers such that once reordered, the value for $|I(k) - I(k-nL)|$ is not evenly divisible by L, where $L = 2^m-1$, and n is a positive integer subject to $k-nL \geq 0$ and $nL \leq S$.

2. The encoder of claim 1 further comprising a tail bit generator for generating a set of tail bits for said encoded input bit set to reset both said registers.

3. The encoder of claim 2 wherein said tail bit generator generates said tail bit sets using the register of said first encoder when the encoding by said first and second encoders is complete.

4. The encoder of claim 1 wherein said interleaver randomly reorders the integers $I(k)$ such that $|I(k) - I(k-j)| > S$ and j is a positive integer defined as $0 < j \leq S$ and $k-j \geq 0$.

5. The encoder of claim 4, wherein the reordered integer I(k) sequence is verified with the following:

$$k \bmod 2^m - 1 = I(k) \bmod 2^m - 1.$$

6. The encoder of claim 1, whereby d_k is an input bit of said set of N bits and where $d_k = \pm 1$, said interleaver further comprising:

means for arranging said input bit sets for an M state turbo code encoder into p disjoint subsets S_i, of size b, where $p = M-1$, i is an integer from 0 to $(p-1)$, b is the smallest integer value larger than or equal to N/p and $S_i = \{d_k, k \bmod p = i\}$;

means for combining subsets S_i, to form a block of b rows and p columns where k is an integer from 1 to b such that each element of a subset is in the same column;

means for reordering the set of input bits within said columns; and

means for outputting said rows after said column reordering to produce an interleaver reordered input bit set.

7. A transmitter having a turbo code encoder for encoding at least one input set of N ordered permutation integers I(k) prior to transmission, where k=1 to N, comprising:

a first encoder with memory size m, having a first input, coupled to a first source and a common source, and a multi-state register having 2^m states, for receiving said input bit set as said first source and encoding said input bit set to provide an encoded input bit set at a first output;

an S-random interleaver for receiving said input bit set and reordering the bits within said input bit set to provide a reordered input bit set, where S is an arbitrary predetermined value;

a second encoder with memory size m, having a second input, coupled to a second source and said common source, and a multi-state register having 2^m states, for receiving said reordered input bit set as said second source and encoding said reordered input bit set to provide a reordered encoded input bit set at a second output; and

a switch, for switching said first encoder from said first source to said common source and for switching said second encoder from said second source to said common source; whereby said first output provides said common source;

whereby said interleaver reorders said integers such that once reordered, the value for $|I(k) - I(k-nL)|$ is not evenly divisible by L, where $L = 2^m-1$, and n is a positive integer subject to $k-nL \geq 0$ and $nL \leq S$.

8. The transmitter of claim 7, whereby the encoder further comprises a tail bit generator for generating a set of tail bits for said encoded input bit set to reset both said registers.

9. The transmitter of claim 8, wherein said tail bit generator generates said tail bit sets using the register of said first encoder when the encoding by said first and second encoders is complete.

10. The transmitter of claim 7, wherein said interleaver randomly reorders the integers I(k) for such that $|I(k) - I(k-j)| > S$ and j is a positive integer defined as $0 < j \leq S$ and $k-j \geq 0$.

11. The transmitter of claim 10, wherein the reordered integer I(k) sequence is verified with the following:

$$k \bmod 2^m - 1 = I(k) \bmod 2^m - 1.$$

12. The transmitter of claim 7, where d_k is an input bit of said set of N bits and $d_k = \pm 1$; and whereby said interleaver further comprises:

means for arranging said input bit sets for an M state turbo code encoder into p disjoint subsets S_i, of size b, where $p = M-1$, i is an integer from 0 to $(p-1)$, b is the smallest integer value larger than or equal to N/p and $S_i = \{d_k|, k \bmod p = i\}$;

means for combining subsets S_i, to form a block of b rows and p columns where k is an integer from 1 to b such that each element of a subset is in the same column;

means for reordering the set of input bits within said columns; and

means for outputting said rows after said column reordering to produce an interleaver reordered input bit set.

13. A turbo code encoder for encoding at least one input set of N ordered permutation integers $I(k)$, where $k=1$ to N, comprising:

a first encoder with memory size m, having a first input, coupled to a first source and a common source, and a multi-state register having 2^m states, for receiving said input bit set as said first source and encoding said input bit set to provide an encoded input bit set at a first output;

an interleaver for receiving said input bit set and reordering the bits within said input bit set to provide a reordered input bit set;

a second encoder with memory size m, having a second input, coupled to a second source and said common source, and a multi-state register having 2^m states, for receiving

said reordered input bit set as said second source and encoding said reordered input bit set to provide a reordered encoded input bit set at a second output; and

a switch, for switching said first encoder from said first source to said common source and for switching said second encoder from said second source to said common source; whereby said first output provides said common source;

whereby said interleaver reorders said integers such that once reordered, the value for $|I(k) - I(k-nL)|$ is not evenly divisible by L, where $L = 2^m-1$, n is a positive integer subject to $k-nL \geq 0$ and $nL \leq S$, and S is an arbitrary predetermined value.